Low Power HFET Down Converter MMIC's for Wireless Communication Applications

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***Abstract*— An ultra low power GaAs HFET (heterojunction FET) amplifier/mixer MMIC was designed and characterized for portable communication applications in the 900 MHz band. A completely monolithic LNA (80 mil × 42 mil) achieved 10 dB gain, 2.5 dB NF and −4 dBm input IP3 at an operating current of 0.5 mA @ 1.0 V. Receiver sensitivity of a front-end circuit consisting of the LNA and a dual gate FET mixer was characterized using the 12 dB SINAD method. The IC achieved −117 dBm receiver sensitivity in the 900 MHz cellular band. The total power consumption of this miniature down converter was about 2 mW. The HFET down converter IC achieved the same receiver sensitivity as a MESFET down converter at 1/5th of the power. The extremely low power dissipation, high third order intercept point, high level of integration, and very good RF performance of this monolithic IC make it an ideal candidate for wireless applications.**

I. Introduction

IN RECENT YEARS GaAs FET's (MESFET's and HEMT's), with their superior noise figure and gain characteristics, have become the device of choice for millimeter-wave, microwave, UHF and VHF *monolithic* circuits. Receiver front-end IC's for portable communication systems such as cellular phones, pagers and portable radios are another area for potential utilization of GaAs technology. GaAs MMIC receivers in wireless communication products lead to a reduction in the number of parts and interconnects and, hence, the size and weight. However, to conserve the battery drain in portable units, devices and circuits have to be designed to operate at very low current levels. Enhancement mode and depletion mode MESFET MMIC amplifiers with excellent RF performance at low current levels have been published [1]–[6]. This paper reports on the development of a low power GaAs HFET MMIC down converter for wireless communication applications.

II. Device Design and Processing

The device structures were grown by MBE on LEC semi-insulating GaAs substrates. The structure consisted of a GaAs/AlAs buffer layer followed by an $In_{0.15}Ga_{0.85}As$ channel layer. An $Al_{0.24}Ga_{0.76}As$ supply layer with Si planar doping was grown on top of the channel. A heavily doped GaAs cap layer was grown for ohmic contact. The processing included Ni/Ge/Au ohmics on GaAs, 0.7 μm Ti/Al Schottky gate on $Al_{0.24}Ga_{0.76}As$ and two level metal interconnects. The buffer layer growth and design were optimized to minimize the buffer layer leakage current for improved transconductance at very low current levels. Fig. 1 shows the transconductance of an HFET and ion implanted MESFET as a function of the device width for 0.5 mA of current. GaAs MESFET was also fabricated in our laboratory using a planar process developed in house. The implantation energy and dose were adjusted to achieve the best performance at low current levels. HFET devices had approximately twice the transconductance of a MESFET for a given gate width and the transconductance at 0.5 mA improved as the device width got smaller to 50 μm. Fig. 2 shows the maximum gain comparison between the nominal 0.7 μm gate length HFET and ion implanted MESFET's as a function of drain current at 2 GHz. The HFET achieved the same gain as an ion implanted MESFET at one-half the current level. For MMIC fabrication, on-chip Si_3N_4 MIM capacitors, dielectric crossovers, and 3 μm thick Au inductors were employed. Low noise amplifier and mixer chips fabricated using this MMIC process are shown in Fig. 3(a) and (b).

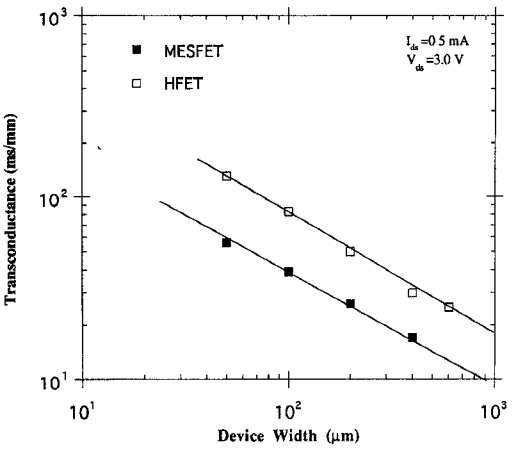

Fig. 1. Transconductance dependence of MESFET and HFET on device width at low currents.

III. Circuit Design

The design goal was to demonstrate a low power integrated front-end technology for wireless applications. Improving the intermodulation characteristics of the low power amplifier was also an important goal. A down converter operating at 1.0 V with less than 2 mA operating current was chosen as the demonstration vehicle. It consisted of a single stage GaAs HFET low noise amplifier (LNA) and a dual gate FET mixer as shown in Fig. 4(a) and (b). A lumped element LC matching network was employed in the design to achieve

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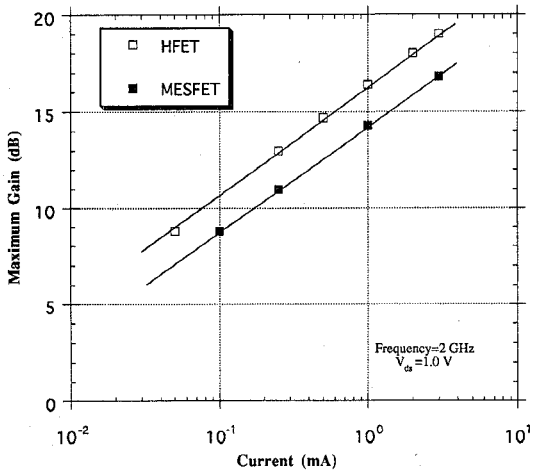
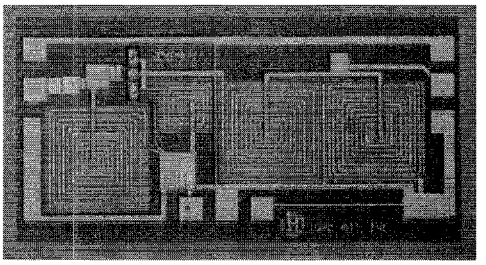
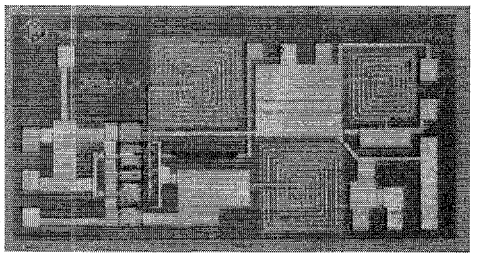


Fig. 2. Maximum gain of a MESFET & HFET device (size = 0.7 μm × 50 μm).



(a)



(b)

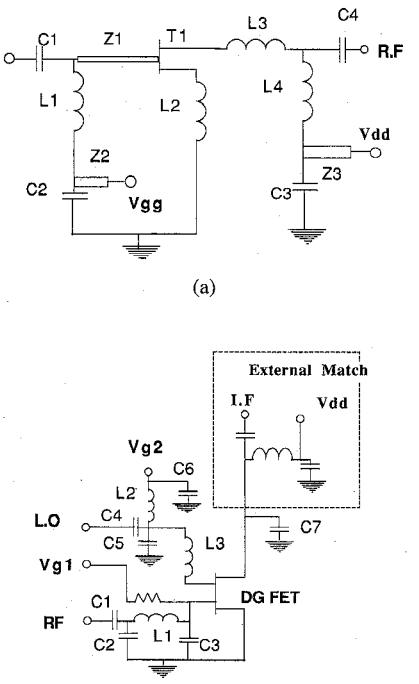
Fig. 3. (a) Fabricated low noise amplifier MMIC chip. (b) Fabricated dual gate FET mixer chip.

on-chip selectivity. The noise parameters of the HFET were measured at very low current levels. A 400 μm HFET achieved 0.8 dB noise figure at an operating current of 0.5 mA at 1.0 V. Single stage amplifiers were modeled using different gate width devices to study the IP3-gain-NF-return loss tradeoff. In order to improve the input third order intercept point of low power LNA's, device harmonics were measured at low frequencies [7]. The circuit IP3 was modeled by representing the device nonlinearities in Volterra series [8]. The circuit was optimized to give high IP3, good frequency response, and good return loss, while maintaining unconditional stability.

IV. Results and Discussion

A. Low Noise Amplifier

The monolithic LNA consisted of a 100 μm HFET with on-chip input and output matching. The gain, IP3, return loss,



(a)

(b)

Fig. 4. (a) Low noise amplifier MMIC schematic. (b) Dual gate FET mixer schematic.

and noise figure were measured on-wafer using an integrated test system developed in-house. The measured gain, IP3, and noise figure of the amplifier are plotted in Fig. 5. This amplifier achieved a gain of 10 dB and noise figure of 2.5 dB at operating current of 0.5 mA and 1.0 V supply voltage. At this low bias point, the amplifier also exhibited very high input IP3 of −4.0 dBm. In Fig. 6, this amplifier performance is compared with published results of other MMIC LNA's. The published literature data on low noise amplifiers that have on-chip matching and at least 10 dB gain were included in this plot. To our knowledge, this MMIC amplifier is the lowest power consumption amplifier reported to date.

B. Dual Gate FET Mixer

A dual gate HFET mixer design was accomplished by using a cascoded connection of two single gate HFET's. RF and L.O. ports were matched on-chip, while the IF port was matched externally to the chip. Fig. 7 shows the conversion loss of the DG mixer as a function of the second gate voltage for various current levels. The mixer performance showed a strong dependence on the voltage applied to the second gate. This monolithic mixer achieved a conversion gain of −0.2 dB at 1.0 mA. When the current was increased to 5 mA the conversion gain of the mixer increased to 8 dB. As the operating current is increased, the second gate voltage at which the maximum conversion efficiency occurs also increased. The optimized second gate voltage was used in the down converter test described below.

C. Down Converter IC

In order to evaluate the performance of the HFET LNA and mixer IC, the MMIC chips were assembled in ceramic

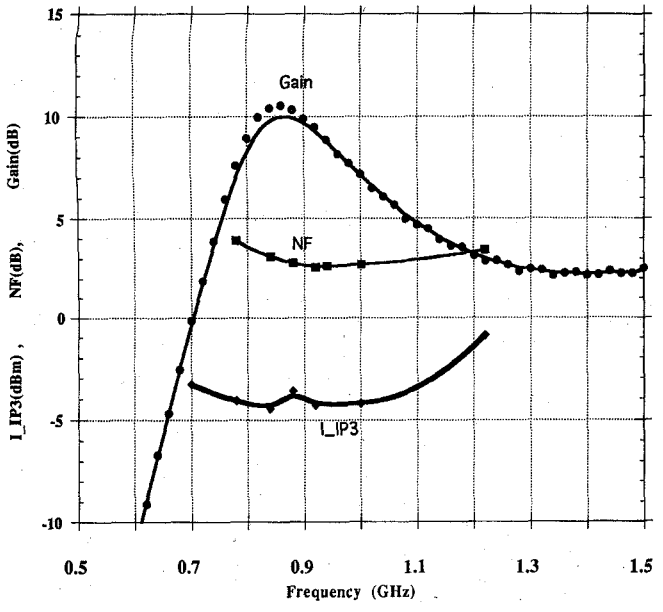


Fig. 5. Measured performance for MMIC low noise amplifier $V_{ds} = 1.0$ V, $I_{ds} = 0.5$ mA.

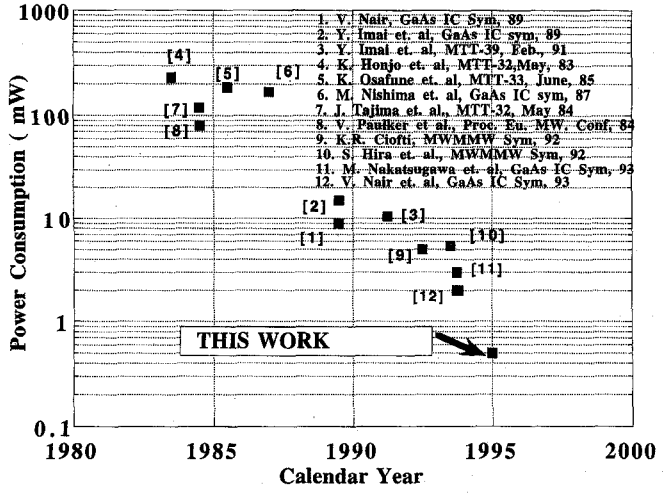


Fig. 6. MMIC low noise amplifier power consumption (LNA's with on-chip matching and Gain $\geq$ 10 dB are included).

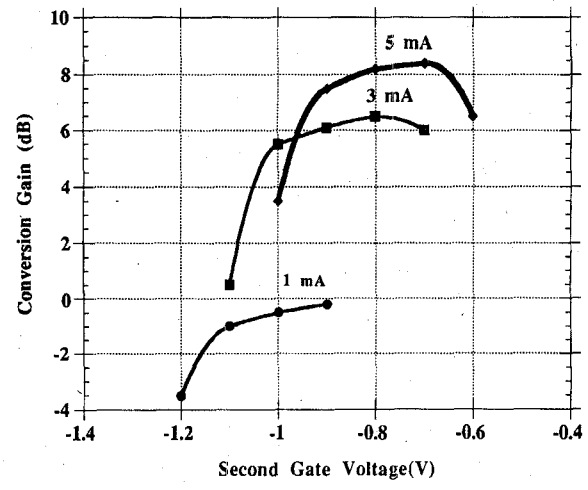


Fig. 7. Dual gate mixer conversion gain as a function of second gate voltage.

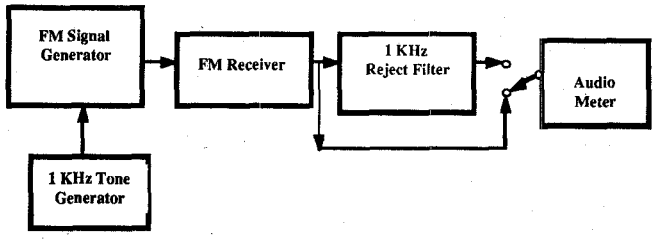


Fig. 8. SINAD Measurement technique.

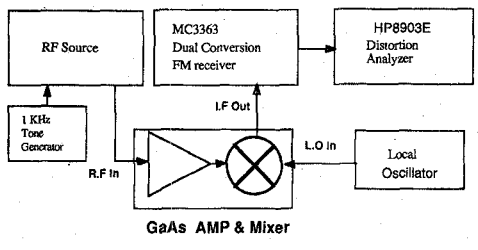


Fig. 9. SINAD Measurement setup.

packages. A complete receiver system was built using the HFET LNA and mixer IC cascaded with a narrow band FM double conversion receiver IC (MC3363DW) and an audio amplifier (MC34119D). The receiver sensitivity of the HFET down converter was measured using the 12 dB SINAD method. This test has been widely adopted by the telecommunications industry as the best way to measure receiver sensitivity. A typical configuration of a SINAD (SIgnal, Noise, And Distortion) measurement setup is shown in Fig. 8. Certain standards to be used in performing the SINAD test have been prescribed in Ref. [9]. An RF signal from the signal generator is frequency modulated by a 1 kHz tone from the audio generator and the modulated signal is fed into the receiver. The amplitude of the composite audio output (consisting of the original modulating tone, the noise components and distortion components) is measured. The composite signal is also fed to a filter which effectively removes the 1 kHz signal component. This filtered output consisting of the sum of the noise and distortion components is then measured. The ratio of the composite audio signal to the noise plus distortion component is computed as the SINAD ratio. When this ratio is 4 (or 12 dB) the noise plus distortion component is 25% of the composite signal. The RF signal level that produces a SINAD of 12 dB is defined as the sensitivity of the receiver. A receiver sensitivity measurement setup, shown in Fig. 9, consists of a distortion analyzer, FM signal generator and a 1 kHz audio generator. Interfacing the 1st IF output of the dual gate HFET mixer to the back end narrow band receiver is accomplished using bandpass interstage matching networks with the on-board transistor preamplifier in the narrow band receiver MC3363DW (see Fig. 10). The MC3363DW narrow band receiver has excellent sensitivity at 45 MHz (12 dB SINAD of better than -119 dBm).

The GaAs down converter was biased at $V_{dd} = 1.2V_{dc}$ and the receiver sensitivity was measured for different mixer and

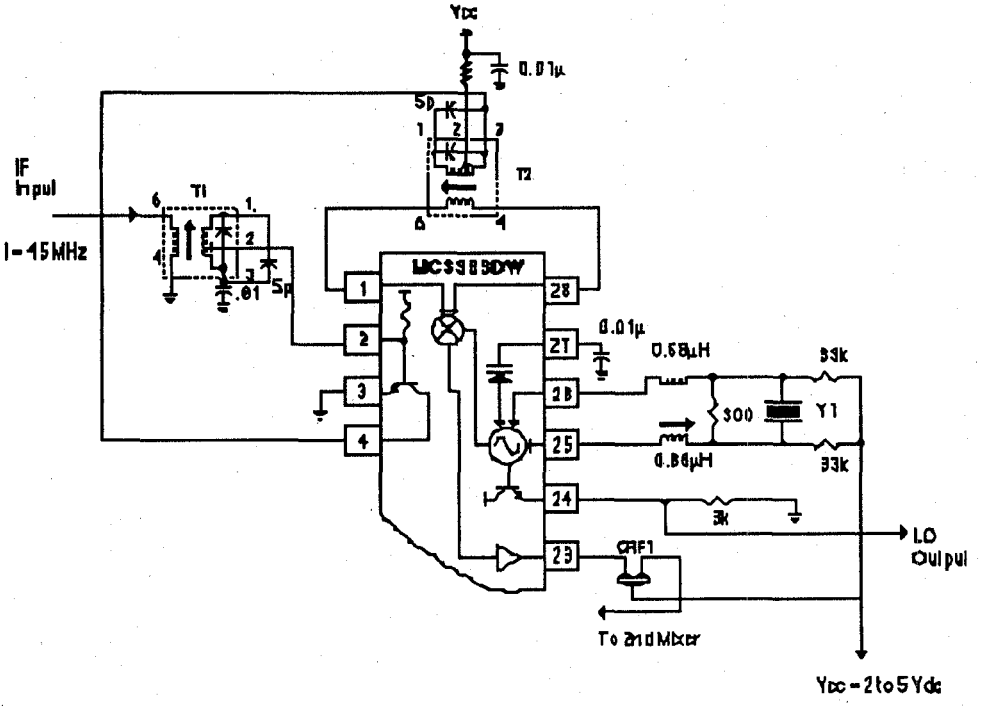


Fig. 10. Second IF circuit for receiver sensitivity measurement.

amplifier currents for different L.O. voltages. In Fig. 11 the receiver sensitivity is plotted as a function of the total current (amplifier plus mixer current, for two different values of mixer current at a L.O. power of −6.0 dBm. When down converter was tested at current levels below 1.5 mA, it achieved better sensitivity at mixer current = 0.5 mA(Case A) compared to that at mixer current = 0.75 mA (Case B). When the mixer current was held at 0.75 mA, the LNA was operated at lower bias point to keep the total down converter current same. Therefore LNA had poorer noise figure and linearity in Case B compared to Case A. This resulted in receiver sensitivity deterioration for Case B. When the total current was above 1.5 mA the dependence of the receiver sensitivity on the mixer current was diminished as shown in Case A and BHFET MMIC down converter achieved a receiver sensitivity of − 117 dBm at 2 mW of power. **This is an 80% reduction in power consumption compared to a MESFET down converter [10].**

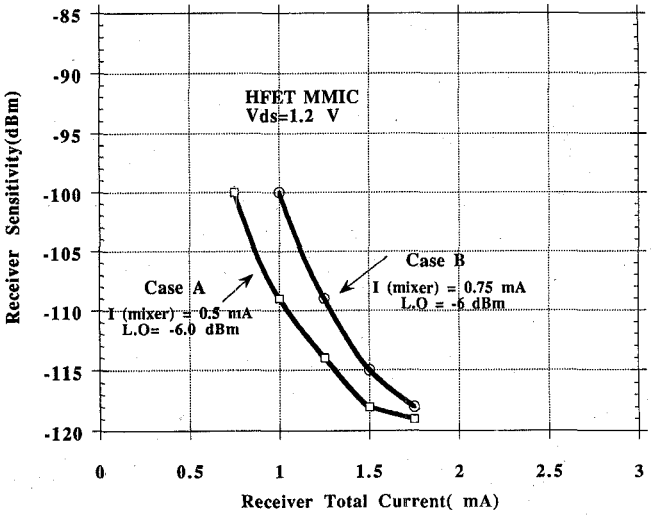


Fig. 11. HFET down converter sensitivity at cellular band.

V. Conclusion

A fully monolithic GaAs HFET MMIC amplifier and mixer was designed, fabricated and tested for potential application in wireless communication system. The total power dissipation of the miniaturized IC was only about 2 mW. This integrated front-end IC achieved −117 dBm sensitivity in the 900 MHz cellular band. The HFET down converter IC achieved same receiver sensitivity as a MESFET down converter at 1/5th of the power. The extremely low power dissipation, high level of integration and very good RF performance of this monolithic IC make it an ideal candidate for portable communication applications.

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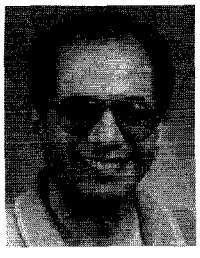
Vijay K. Nair (SM'91) for a photograph and biography, see this issue p. 2725.



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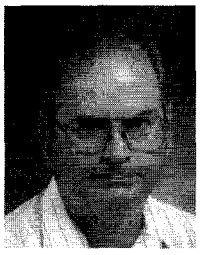

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